LISTING OF THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Claims 1-21 (Cancelled)

22. (NEW) A MOSgated device comprising:

a semiconductor body of a first conductivity type;

a channel region of a second conductivity type formed in said semiconductor body;

a conductive region of said first conductivity type formed in said semiconductor body and extending from a first major surface of said semiconductor body to at least said channel region;

a plurality of spaced trenches extending into said semiconductor body below said channel region, each of said trenches being adjacent a mesa and each terminating at a contact region in said semiconductor body, said channel region and said conductive region extending into said contact region, and said conductive region uninterruptedly extending between each two adjacently disposed trenches;

a gate insulation layer dispose over the sidewalls and bottom of each of said trenches;

a gate electrode formed in each of said trenches over said gate insulation layer;

at least one conductive strip extending transverse to each of said trenches and electrically connected to each of said gate electrodes; said conductive strip being narrow such that it makes contact only with a portion of each of said gate electrodes; and

a remote contact formed over at least said contact region and in electrical contact with at least said conductive region.

23. (NEW) A MOSgated device according to claim 22, wherein said remote contact extends through said conductive region to make contact with said channel region below said conductive region.

24. (NEW) A MOSgated device according to claim 22, wherein said conductive region is a source region.

25. (NEW) A MOSgated device according to claim 22, wherein said gate electrode comprises conductive polysilicon.

26. (NEW) A MOSgated device according to claim 22, wherein said gate insulation layer comprises an oxide.

27. (NEW) A MOSgated device according to claim 22, wherein said semiconductor body is an epitaxial silicon layer formed over a silicon substrate of the same conductivity and further comprising a second contact in electrical contact with said substrate.

28. (NEW) A MOSgated device according to claim 27, wherein said second contact is a drain contact.

29. (NEW) A MOSgated device according to claim 22, wherein said remote contact is a source contact.

30. (NEW) A MOSgated device according to claim 22, wherein said plurality of spaced trenches are parallel to one another and are coextensive with one another.

31. (NEW) A MOSgated device according to claim 22, wherein said plurality of spaced trenches are formed in a plurality of spaced rows and are parallel to one another and are coextensive with one another within each row.

32. (NEW) A MOSgated device according to claim 22, wherein said trenches have a depth of about 1.8 microns.

33. (NEW) A MOSgated device according to claim 22, wherein said trenches extend to about 0.2 to 0.25 microns below said channel region.

34. (NEW) A MOSgated device according to claim 22, wherein said trenches have a width of about 0.6 microns and a spacing of about 0.6 microns or greater.

35. (NEW) A MOSgated device according to claim 22, wherein said gate insulation is an oxide layer having a thickness greater than about 200 Å and which fully covers the interior of each of said trenches.

36. (NEW) A MOSgated device comprising:

an epitaxial silicon body of a first conductivity type;

a channel region of a second conductivity type formed in said epitaxial silicon body;

a source region of said first conductivity type formed in said epitaxial silicon body and extending from a first major surface of said silicon body to at least said channel region;

a plurality of spaced trenches extending into said silicon body below said channel region, each of said trenches being adjacent a mesa and each terminating at a source contact region in said silicon body, said channel region and said source region extending into said source contact region, and said source region uninterruptedly extending between each two adjacently disposed trenches;

a gate oxide layer dispose over the sidewalls and bottom of each of said trenches;

a polysilicon gate electrode formed in each of said trenches over said gate oxide layer;

at least one conductive strip extending transverse to each of said trenches and electrically connected to each of said polysilicon gate electrodes; said conductive strip being narrow such that it makes contact only with a portion of each of said polysilicon gate electrodes; and

a remote source contact formed over at least said source contact region and in electrical contact with at least said source region.

37. (NEW) A MOSgated device according to claim 36, wherein said remote source contact extends through said source region to make contact with said channel region below said source region.

38. (NEW) A MOSgated device according to claim 36, further comprising a silicon substrate and a drain contact in electrical connection with said substrate, said epitaxially silicon substrate being formed over said substrate.

39. (NEW) A MOSgated device according to claim 36, wherein said plurality of spaced trenches are parallel to one another and are coextensive with one another.

40. (NEW) A MOSgated device according to claim 36, wherein said plurality of spaced trenches are formed in a plurality of spaced rows and are parallel to one another and are coextensive with one another within each row.

41. (NEW) A MOSgated device according to claim 36, wherein said trenches have a depth of about 1.8 microns.

42. (NEW) A MOSgated device according to claim 36, wherein said trenches extend to about 0.2 to 0.25 microns below said channel region.

43. (NEW) A MOSgated device according to claim 36, wherein said trenches have a width of about 0.6 microns and a spacing of about 0.6 microns or greater.